Project Description

This project was aimed at providing people a simple, runnable, and easy-to-enhance MIPS CPU main architecture, along with well commented Verilog RTL source code, complete simulation test benches & scripts, and detailed documentation. People can read the source code, make simulations to verify the result, and then make modifications to enhance it. I hope this project can help you learning the MIPS CPU architecture and enjoy constructing your own CPU core.

This CPU design is based on Mr. Hu Weiwu’s book ”Computer Achitecture”, Tsinghua University Press, 2011